Notice of Allowability	Application No.	Applicant(s)	
	10/763,136	FORBES ET AL.	
	Examiner	Art Unit	
	Tuan T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE filed on 12/13/04*.

2. ☒ The allowed claim(s) is/are *1-54*.

3. ☒ The drawings filed on *22 January 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 12/13/04, 12/27/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

4/24/05

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

1. This is the response to the Applicant's RCE filed on 12/13/04.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 12/13/04 and 12/27/04 were filed after the mailing date of the present application. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

3. Claims 1-54 are allowed.

4. The following is an examiner's statement of reasons for allowance:

The prior art of record fail to disclose a programmable element comprising the gate oxide having an electron charge trapped in the gate oxide adjacent to the first source/drain region and substantially no charge trapped in the gate oxide adjacent to the second source/drain region, the amount of electron charge trapped in the gate oxide adjacent to the first source/drain region is sufficient to cause the conduction channel to have at least two different voltage threshold regions as recited in claims 1-6, 7-11.

The prior art of record fail to disclose a programmable element comprising a non-volatile memory cell comprising a semiconductor element having a conductive gate located adjacent to and separated from the channel region by a charge trapping insulator such that the channel region has a first voltage threshold (Vt1) in a first portion of the channel and a second voltage threshold (Vt2) in a second portion of the channel region as recited in claims 12-14.

The prior art of record fail to disclose a programmable element comprising programmable memory element, comprising the transistor having a first programmed state whereby electrons are injected into the gate oxide by avalanche hot electron injection; and the transistor having a second programmed state whereby the electrons are re-emitted back into the channel region as recited in claims 15-17.

The prior art of record fail to disclose a non-volatile memory, comprising wherein the charge trapping element is a programmable device having a charge trapped in the gate oxide adjacent to the source region and substantially no charge trapped in the gate oxide adjacent to the drain region such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2) as recited in claims 18-23, 24-25, 26-27.

The prior art of record fail to disclose a method of programming a non-volatile memory cell, comprising applying a first voltage (V1) to a first source/drain terminal of a transistor; applying a second voltage (V2) to a second source/drain terminal of the transistor, where the second voltage is greater than the first voltage; applying a gate voltage sufficient to turn on a channel of the transistor; and injecting electrons into a gate oxide of the transistor adjacent to the first source/drain region but not adjacent to the second source/drain region as recited in claims 28-30.

The prior art of record fail to disclose a method of using a transistor as a non-volatile memory cell comprising operating the transistor in a reverse direction to program the transistor by avalanche hot electron injection from a channel of the transistor to trap electrons in the gate oxide adjacent to a source of the transistor resulting in a programmed transistor as recited in claims 31-37.

The prior art of record fail to disclose a method of utilizing a MOSFET as a memory cell comprising operating the MOSFET in a reverse direction to trap electrons in a source end of a gate oxide of the MOSFET to cause the channel to have at least two different threshold voltage regions as recited in claims 38-41.

The prior art of record fail to disclose a method of using a normal MOSFET as a memory cell, comprising programming the MOSFET by operation in the reverse direction and utilizing avalanche hot electron injection to trap electrons in the gate oxide of the MOSFET causing a channel of the VOSFET to have two different threshold voltage regions; and reading the programmed MOSFET by operating the MOSFET in the forward direction to sense the electrons trapped in the oxide near a source of the MOSFET as recited in claims 42-48.

The prior art of record further fail to disclose a method of operating a transistor as a non-volatile memory cell, comprising applying a first voltage to a drain terminal of the transistor; applying a second voltage to a source terminal of the transistor, where the second voltage is greater than the first voltage; injecting electrons from a channel of the transistor into a gate oxide of the transistor; applying a third voltage to the drain terminal of the transistor; applying a fourth voltage to the source terminal of the transistor, where the third voltage is greater than the fourth voltage; and sensing the electrons trapped in the gate oxide of the transistor as recited in claims 49-51.

The prior art of record further fail to disclose a method of operating a MOSFET as a non-volatile memory cell comprising operating the MOSFET in a reverse direction to trap electrons in a source end of a gate oxide of the MOSFET to cause the channel to have at least two different

threshold voltage regions; and operating the MOSFET in a forward direction to sense the trapped electrons in the source end of the gate oxide of the MOSFET as recited in claims 52-54.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Nguyen whose telephone number is (571) 272-1880. The examiner can normally be reached on Mon-Thu-Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 24, 2005

Tuan T. Nguyen
Patent Examiner
Art Unit 2824